IN THE CLAIMS

Please amend the claims as follows:

Claims 1-20 (Canceled).

Claim 21 (New): A parallel processor for processing a plurality of operation instructions in one cycle in parallel, comprising:

a first operation processor; and

at least one second operation processor which runs by an extended instruction supplied from the first operation processor, wherein the extended instruction includes a first code for the first operation processor and a second code for the second operation processor,

the first operation processor including,

a control unit for, in case that an operation mode indicating whether or not the second operation processor should be run in parallel to carry out an operation instruction is a first operation mode, in accordance with the operation mode, supplying the first operation processor with an instruction sequence that defines an operation of the first operation processor, and for generating a control signal to halt an operation of the second operation processor and supplying the control signal to the second operation processor, and

an instruction execution unit for switching the operation mode in accordance with an input decoded instruction,

wherein the operation mode has a first operation mode in which the first operation processor alone is operated, and a second instruction mode in which both of the first operation processor and the second operation processor are operated, and

the extended instruction comprises only the first code in the first operation mode.

Claim 22 (Previously Presented): The parallel processor according to claim 21, wherein in case that the operation mode is the second operation mode, the control unit supplies the first operation processor with an instruction string that defines an operation of the first operation processor, and supplies the second operation processor with an instruction string that defines an operation of the second operation processor.

Claim 23 (Previously Presented): The parallel processor according to claim 21, wherein the control signal is a no operation instruction.

Claim 24 (Previously Presented): The parallel processor according to claim 21, wherein in the first operation mode, the instruction sequence retained in an instruction memory includes only an instruction that defines an operation of the first operation processor.

Claim 25 (Previously Presented): The parallel processor according to claim 23, wherein the control unit includes a no operation instruction retaining unit for retaining the no operation instruction; and in the first operation mode, the instruction string retained in the instruction memory constantly includes a plurality of instructions.

Claim 26 (Previously Presented): The parallel processor according to claim 21, wherein the control signal is a signal that stops a supply of a clock to the second operation processor.

Claim 27 (Previously Presented): The parallel processor according to claim 21, wherein the control signal is a disable signal of the second operation processor.

Claim 28 (Previously Presented): The parallel processor according to claim 21, wherein the instruction execution unit switches the operation mode by executing a sub-routine call instruction directing an operation mode switching.

Claim 29 (Currently Amended): The parallel processor according to claim 28, wherein:

the control unit includes a first return address register for retaining a return address from the sub-routine call instruction;

the instruction execution unit, when executing the sub-routine call instruction, switches a value of the operation mode, and sets information indicating inversion of the operation mode in the first return address register, and

when returning from the sub-routine call instruction, refers to the information indicating the inversion of the operation to the information indicating the inversion of the operation mode set in the first return address register, and if the inversion is set, returns to the operation mode set before the sub-routine call instruction by inverting the value of the operation mode set in the first return address register.

Claim 30 (Previously Presented): The parallel processor according to claim 21, wherein the instruction execution unit switches the operation mode at an occurrence of an exception.

Claim 31 (Previously Presented): The parallel processor according to claim 30, wherein:

the control unit includes a second return address register for retaining a return address from an exception handling program by which the exception handling is carried out;

the instruction execution unit, at an occurrence of the exception, switches the operation mode by inverting the value of the operation mode, and sets information indicating inversion of the operation mode in the second return address register, and

when returning from the exception, refers to the information indicating the inversion of the operation mode set in the second return address register, and if the inversion is set, returns to the operation mode set before the exception by inverting the value of the operation mode.

Claim 32 (Previously Presented): The parallel processor according to claim 21, wherein the instruction execution unit switches the operation mode by inverting the value of the operation mode in accordance with information indicating inversion of the operation mode contained in a part of a jump address defined in a jump instruction.

Claim 33 (Previously Presented): The parallel processor according to claim 21, wherein the second operation processor comprises a plurality of coprocessors; and

the control unit, in the first operation mode, operates the first operation processor alone by stopping clocks to the plurality of coprocessors other than the first operation processor.

Claim 34 (Previously Presented): The parallel processor according to claim 21, wherein the control unit supplies the control signal to, in accordance with an extended operation mode indicating which of a plurality of second operation processors should be operated to carry out the operation instruction in parallel, the remaining second operation processor other than the second operation processor which is indicated by the extended operation mode.

Claim 35 (Previously Presented): The parallel processor according to claim 21, wherein the instruction supplied by the control unit is a single instruction stream multiple data stream (SIMD) instruction.

Claim 36 (Previously Presented): The parallel processor according to claim 21, wherein the first operation processor is an integer processor and the second operation processor is a data processor.

Claim 37 (Previously Presented): The parallel processor according to claim 36, wherein the instruction sequence is 64-bit length and includes a first portion for the integer processor and a second portion for the data processor.

Claim 38 (Previously Presented): The parallel processor according to claim 21, further comprising an instruction register unit including:

an instruction register for retaining the instruction sequence which is either an instruction string for the first operation processor alone or an instruction string for the first and second operation processors; and

a selector for supplying the first operation processor with a part of the instruction sequence retained by the instruction register.

Claim 39 (Currently Amended): A computer system equipped with a parallel processor for processing more than one operation instruction in one cycle, comprising:

a first operation processor;

at least one second operation processor which runs by an extended instruction supplied from the first operation processor, wherein the extended instruction includes a first code for the first operation processor and a second code for the second operation processor; and

a data memory,

the first operation processor including,

a control unit for, in case that an operation mode indicating whether or not the second operation processor should be run in parallel to carry out an operation instruction is a first operation mode, in accordance with the operation mode, supplying the first operation processor with an instruction sequence that defines an operation of the first operation processor, and for generating a control signal to halt an operation of the second operation processor and supplying the control signal to the second operation processor, and

an instruction execution unit for switching the operation mode in accordance with an input decoded instruction,

wherein the operation mode has a first operation mode in which the first operation processor alone is operated, and a second instruction mode in which both of the first operation processor and the second operation processor are operated, and

the extended instruction comprises only the first code in the first operation mode.

Claim 40 (Previously Presented): The computer system according to claim 39, wherein in case that the operation mode is the second operation mode, the control unit supplies the first operation processor with an instruction string that defines an operation of the first operation processor, and supplies the second operation processor with an instruction string that defines an operation of the second operation processor.

Claim 41 (Previously Presented): The computer system according to claim 39, wherein the control signal is a no operation instruction.

Claim 42 (Previously Presented): The computer system according to claim 39, wherein in the first operation mode, the instruction sequence retained in an instruction memory includes only an instruction that defines an operation of the first operation processor.

Claim 43 (Previously Presented): The computer system according to claim 42, wherein the control unit includes a no operation instruction retaining unit for retaining the no operation instruction; and

in the first operation mode, the instruction string retained in the instruction memory constantly includes a plurality of instructions.

Claim 44 (Previously Presented): The computer system according to claim 39, wherein the control unit supplies the control signal to, in accordance with an extended operation mode indicating which of a plurality of second operation processors should be operated to carry out the operation instruction in parallel, a remaining second operation processor other than the second operation processor which is indicated by the extended operation mode.

Claim 45 (Previously Presented): The computer system according to claim 39, wherein the instruction supplied by the control unit is a single instruction stream multiple data stream (SIMD) instruction.

Claim 46 (Previously Presented): The computer system according to claim 39, wherein the first operation processor is an integer processor and the second operation processor is a data processor.

Claim 47 (Previously Presented): The computer system according to claim 46, wherein the instruction sequence is 64-bit length and includes a first portion for the integer processor and a second portion for the data processor.

Claim 48 (Previously Presented): The computer system according to claim 39, further comprising an instruction register unit including:

an instruction register for retaining the instruction sequence which is either an instruction string for the first operation processor alone or an instruction string for the first and second operation processors; and

a selector for supplying the first operation processor with a part of the instruction sequence retained by the instruction register.

Claim 49 (Currently Amended): A method for operating a parallel processor for processing a plurality of operation instructions in one cycle in parallel, comprising:

supplying, in case that an operation mode indicating whether or not a second operation processor should be run in parallel to carry out an operation instruction is a first operation mode, a first operation processor with an instruction sequence that defines an operation of the first operation processor, and generating a control signal to halt an operation of a second operation processor and supplying the control signal to the second operation processor, the second instruction processor running by an extended instruction supplied from

the first operation processor, wherein the extended instruction includes a first code for the first operation processor and a second code for the second operation processor;

supplying, in case that the operation mode is a second operation mode, the first operation processor with an instruction string that defines an operation of the first operation processor, and supplying the second operation processor with an instruction string that defines an operation of the second operation processor; and

switching the operation mode in accordance with an input decoded instruction, wherein the operation mode has a first operation mode in which the first operation processor alone is operated, and a second instruction mode in which both of the first operation processor and the second operation processor are operated, and the extended instruction comprises only the first code in the first operation mode.

Claim 50 (Currently Amended): A parallel processor for processing a plurality of operation instructions in one cycle in parallel, comprising:

a first operation processor; and

at least one second operation processor which runs by an extended instruction supplied from the first operation processor, wherein the extended instruction includes a first code for the first operation processor and a second code for the second operation processor,

the first operation processor including,

a control unit for, in case that an operation mode indicating whether or not the second operation processor should be run in parallel to carry out an operation instruction is a first operation mode, in accordance with the operation mode, supplying the first operation processor with an instruction sequence that defines an operation of the first operation processor, and for generating a control signal to halt an operation of the second operation processor and supplying the control signal to the second operation processor, and

an instruction execution unit for switching an operation mode in accordance with information indicating inversion of the operation mode located by a part of an input decoded instruction,

wherein the operation mode has a first operation mode in which the first operation processor alone is operated, and a second instruction mode in which both of the first operation processor and the second operation processor are operated, and

the extended instruction comprises only the first code in the first operation mode.